IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.:	10/712,736	Confirmation No.: 8891
Appellant:	Cheung et al	
Filed:	11/12/2003	
TC/AU:	2182	
Examiner:	Nguyen	
Docket:	TI-32389.1	
Cust.No.:	23494	

SECOND SUBSTITUTE APPEAL BRIEF

Commissioner for Patents
P.O.Box 1450
Alexandria VA 22313-1450

Sir:

In response to the Notice of Non-Compliant Appeal Brief mailed 08/31/2006, appellant attaches the following sheets which contain the Rule 41.37 items of appellant's second substitute Appeal Brief. The fee for filing a brief in support of the appeal has previously been paid. The Director is hereby authorized to charge any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

/Carlton H. Hoel/

Carlton H. Hoel
Reg. No. 29,934
Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, Texas 75265
972.917.4365

Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Pursuant to MPEP 1205.02, for each claim in the case appellant states the status as follows:

Claim 1: cancelled

Claim 2: cancelled

Claim 3: cancelled

Claim 4: cancelled

Claim 5: cancelled

Claim 6: cancelled

Claim 7: rejected

Claim 8: rejected

Claim 9: rejected

Claim 10: rejected

Claim 11: rejected

Claim 12: cancelled

Claim 13: withdrawn

Claim 14: withdrawn

Claim 15: withdrawn

Claim 16: withdrawn

Claim 17: withdrawn

Claim 18: withdrawn

Claim 19: withdrawn

Claim 20: withdrawn

Pursuant to MPEP 1205.02, appellant identifies each claim on appeal as follows

Claim 7: on appeal

Claim 8: on appeal

Claim 9: on appeal

Claim 10: on appeal

Claim 11: on appeal

Rule 41.37(c)(1)(iv) Status of amendments

There is no claim amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The independent claims on appeal consist of apparatus claim 7.

The subject matter of claim 7 is a serial-peripheral interface (SPI) for use with a microcontroller where the SPI includes a plurality of hardware pointers to memory locations in a FIFO buffer (application page 11, lines 6-7), at least one hardware pointer counter (application page 11, lines 13-14), and a hardware logic device configured to communicate with a bus interface and to utilize the FIFO buffer for intermediate storage of data being transmitted from and received to a CPU (application page 10, lines 13-17) and where the SPI is further configured to communicate with a DMA module and the bus interface (application page 10, lines 2-4) for providing cycle stealing (application page 12, lines 15-17).

As background, claim 7 relates to a serial-peripheral interface (SPI) for a microcontroller which uses a FIFO with separate pointers (and difference counters) for the SPI and the microcontroller in connection with handling microcontroller communications with peripherals; the FIFO is part of the microcontroller's memory and is accessed by the SPI through the microcontroller's DMA using cycle stealing, thereby not loading the microcontroller. Fig.1 shows SPI 108 between the microcontroller bus interface 104 (plus DMA 112) and peripherals 101; the FIFO is in CPU SRAM 106. Fig.2B heuristically illustrates FIFO 208 as a circle of 16 memory locations with SPI pointers SPItxp for transmit and SPIrxp for receive plus microcontroller pointers CPUtxp for transmit and CPUrxp for receive; TXcnt is the transmit difference counter and RXcnt is the receive difference counter. Application paragraphs

[0026] and [0048] describe the cycle stealing, and paragraphs [0028] to [0033] describe the operation of the FIFO and pointers and counters for communications of the microcontroller with peripherals. The SPI essentially buffers microcontroller communications using part of the microcontroller's memory but without loading the microcontroller.

Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

Claims 7-11 were rejected under 35 USC § 103(a) as unpatentable over Hill et al. (US 4,816,996) in view of Sowell et al. (US 5,047,927).

Rule 41.37(c)(1)(vii) Arguments

Claims 7-11 were rejected under 35 USC § 103(a) as unpatentable over Hill et al. (US 4,816,996) in view of Sowell et al. (US 5,047,927).

Claims 7-11: Appellants reply that Hill does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with DMA module and the bus interface for providing cycle stealing (claim 7, last clause). Appellants agree with the Examiner (as evidenced by page 4 of the Office Action) that Hill does not disclose the SPI for providing cycle stealing.

It is respectfully submitted that Sowell also does not disclose or suggest the presently claimed invention including the SPI being further configured to communicate with the DMA module and the bus interface for providing cycle stealing (claim 7, last clause). The Board's attention is directed to column 3, lines 5-10 of Sowell. Here, Sowell discloses that the direct memory access DMA provides a fast means for retrieving and placing data that is required for the HDLC block. The DMA is generally used in a "cycle stealing mode" which provides an efficient means of data movement. Sowell or any prior art reference applied by the Examiner does not disclose a SPI having cycle stealing.

Rule 41.37(c)(1)(viii) Claims appendix

7. A serial peripheral interface (SPI) for use with a microcontroller and configured for increasing the rate of data communications, wherein the SPI module comprises:

a plurality of hardware pointers to memory locations in a FIFO buffer;

at least one hardware pointer counter; and

a hardware logic device; wherein the hardware logic device is configured to communicate with a bus interface and to utilize the FIFO buffer for intermediate storage of data being transmitted from and received to the CPU,

wherein the SPI is further configured to communicate with a DMA module and the bus interface for providing cycle stealing.

8. The SPI of claim 7 wherein the plurality of hardware pointers are configured to provide at least one of a CPU transmitter pointer signal, a CPU receiver pointer signal, a SPI transmitter pointer signal and a SPI receiver pointer signal.

9. The SPI of claim 7 the SPI module further comprising a transmitter buffer and a receiver buffer;

wherein the transmitter buffer is configured to transmit data from the FIFO buffer, and wherein the receiver buffer is configured to transmit data to the FIFO buffer.

10. The SPI of claim 7 the SPI module further configured to operate as one of a master device and a slave device.

11. The SPI of claim 7 the SPI module further configured to provide a data register chip select signal to the bus interface.

Rule 41.37(c)(1)(ix) Evidence appendix

none

Rule 41.37(c)(1)(x) Related proceedings appendix

none